A 1.0V GaAs Receiver Front-end IC for Mobile Communication Equipment

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Abstract

A 1.0V operation GaAs receiver front-end IC has been developed by using novel combination of an E-FET and a D-FET for the amplifiers and mixer, high performance GaAs BP-MESFET and on-chip high-ε_r capacitors. The IC shows conversion gain (CG) of 23dB, noise figure (NF) of 2.8dB, the 3rd order output intercept point (IP3out) of 3dBm, image rejection ratio (IRR) over 20dB and LO to RF isolation over 25dB, operating at 880MHz and 6.8mA. At 1.9GHz, the IC also has excellent RF characteristics at dissipation current of 6.5mA. The IC chip has the small size of 0.75mm x 0.75mm, and is molded in a mini-6pin package.

Introduction

In order to attain the miniaturization, light weight and long standby, which are the greatest concern for a mobile communication equipment, high integration of circuits and low power operation of the RF section must be accomplished at the same time. GaAs MMIC is suitable device for the RF section because of low noise, low dissipation current, high efficiency and high gain. We have already reported on the GaAs front-end IC which integrated LNA, mixer, and LO Amplifier(LOA) with low power operation for small sized cellular telephones[1-6]. In addition, many types of GaAs MMIC down converters with low power consumption have been developed so far[7-8]. However, these ICs need over 2.7V of supply voltage to obtain good RF characteristics and low dissipation current. The purpose of this work is to develop a low voltage and low current receiver front-end IC operating on "one battery cell" (1.2V).

Design of the IC

In order to attain the low voltage operation front-end IC with high RF performance and low dissipation current, next four techniques are developed.

(1) E/D amplifiers and a D/E mixer for low voltage operation.
(2) Intermediate tuned circuit for high gain and high image rejection ratio.
(3) Self-aligned buried p-layer MESFET(BP-MESFET) with 0.5µm refractory metal gate for high gain and low dissipation current.
(4) High ε_r capacitors for integration of the circuits.

A. Amplifiers and Mixer

The most important technique for lowering the supply voltage is the combination of an E-FET and a D-FET for the amplifiers and mixer. Figure 1 shows the basic circuits of the amplifier and mixer.

The amplifiers are composed of a cascode connection of a symmetric E-FET and an asymmetric D-FET. The E-FET lowers the source bias voltage of amplifier and ensures the sufficient voltages between drain and source(Vds) at low voltage operation. In this IC, most part of the supply voltage is mainly applied to source-drain, because of the source bias voltage is about 0.1V. On the other hand, sufficient isolation from the output to input ports is obtained by ac grounding D-FET of the 2nd-satge.

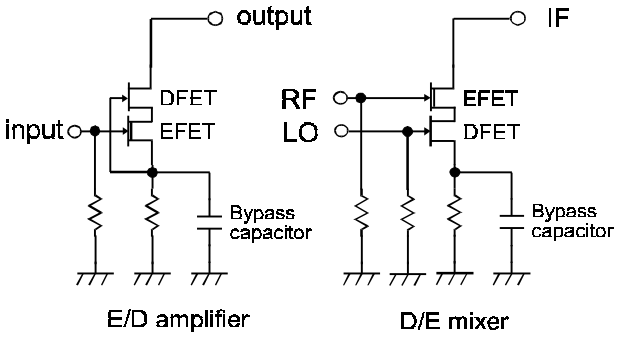

Fig.1 Basic circuits of the amplifier and mixer for the front-end IC

Figure 2 shows a magnitude of S21 and dissipation currents versus supply voltage using E/D amplifier in comparison with the conventional D/D amplifier.

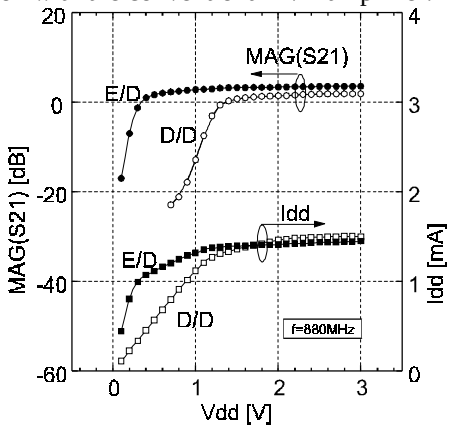

Fig.2 Gain and Ids of the amplifier as a function of supply voltages

The mixer is designed to obtain high conversion gain and high IP3out even at low supply voltage. This circuit is composed of a cascode connection of a symmetric D-FET and an asymmetric E-FET, with both gates biased at 0V. The LO signal is input to the gate of the 1st-stage D-FET, and the RF signal to the gate of the 2nd-stage E-FET. The 1st-stage D-FET is switched by the LO input signal, then the 2nd-stage E-FET switches amplification of the RF signal, as a result, the IF signal is obtained at the drain of the 2nd-stage E-FET. The conversion gain of this type of mixer depends mainly on the ability of amplification of the 2nd-stage E-FET and the completeness of switching operation of the 1st-stage D-FET. The D/E mixer satisfies these two factors at the same time even at low supply voltage. The 2nd-stage E-FET is biased to operate in the linear region to enhance IP3out by applying the most part of the supply voltage, because the 1st-stage D-FET requires much lower Vds for switching operation. By this D/E combination, high IP3out is obtained at only 1.0V of supply voltage.

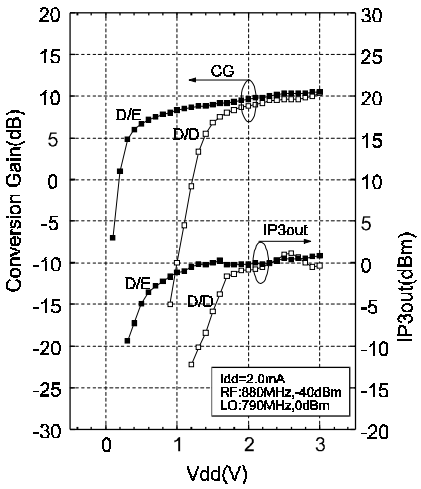

Fig.3 Conversion Gain and IP3out of the mixer as a function of supply voltages

B. Intermediate tuned circuits

The IC is designed to have the ability of image rejection by its intermediate tuned circuit and narrow band input matching circuit of the LNA. The tuned circuit is composed of the external inductor, the input capacitance of the mixer and the output capacitance of the LNA (Fig.5). Image rejection ratio over 20dB is obtained at 880MHz. The LOA and the mixer are connected using the same circuit topology to get high gain and low power consumption.

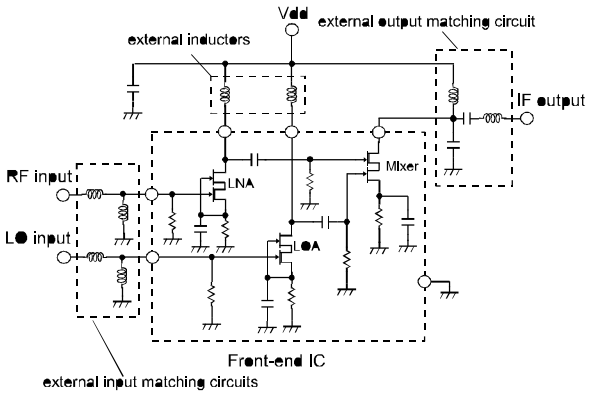

Fig.4 Circuit diagram of the front-end IC

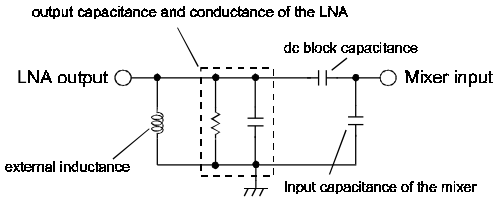

Fig.5 Equivalent intermediate tuned circuit

C. IC process

Figure 6 shows a schematic cross-section of this IC. The GaAs MESFET was fabricated by using the buried p-layer self-aligned LDD(lightly doped drain) process utilizing a refractory metal gate. Gate length(Lg) is 0.5µm. The threshold voltages of E-FET and D-FET are -0.15V and -1.0V, respectively. In order to obtain low drain conductance and high K-value on the asymmetric LDD FET, the distance between the gate and drain is optimized as 1.0µm. The Drain conductance of 0.55mS/mm is obtained at Vds=3V and Vgs=0V. The symmetric LDD FET was designed to have high K-value and low knee voltage. The K-value and knee-voltage of these FETs were,340mA/V^{2}mm, 0.25V for the E-FET and 208mA/V^{2}mm, 0.3V for the D-FET.

The MIM capacitors using the high εr thin films are fabricated by the low-temperature RF sputtered $SrTiO_3$ process technique[9-11]. The film deposition temperature is 300ºC and the thickness of $SrTiO_3$ is 300-nm. εr over 100, leakage current density under 10^{-6}A/cm^2 at 1MV/cm, and the break-down voltage over 30V were obtained without any degradation of the FET. The integration of bypass capacitors on the IC chip made it possible to reduce the parasitic inductance of the source-to-ground interconnections, and to decrease chip size and number of pins. The IC chip has the size of 0.75mm x 0.75mm and molded in a mini-6pin plastic package.

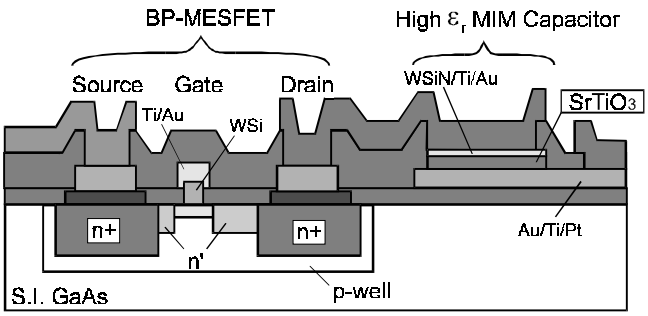

Fig.6 Schematic cross-sectional view of the LDD BP-MESFET

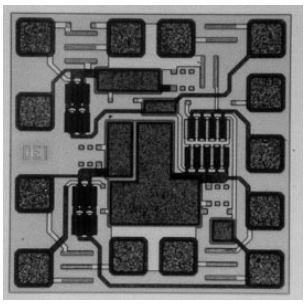

Fig.7 Micro-photograph of the GaAs IC chip

IC Performance

Figure 8 shows CG, IP3out and NF versus the supply voltages (Vdd) of the 880MHz front-end IC in comparison with the conventional IC using D-FETs. Excellent RF characteristics hold out towards 1.0V of supply voltage, while conventional IC deteriorates bellow 2.0V.

Figure 9 shows the LO-power response of the IFout, 3rd-order intermodulation distortion(IM3), dissipation current(Idd), and NF at 1.0V. It is recognized from this figure that 1.0V operation is realized under low LO input power.

Figure 10 shows the frequency response of the CG, image rejection ratio(IRR) and NF at center frequency of 880MHz. This figure shows that sufficient IRR of over 20dB are obtained without external filters by using intermediate tuned circuit and narrow band matching circuit.

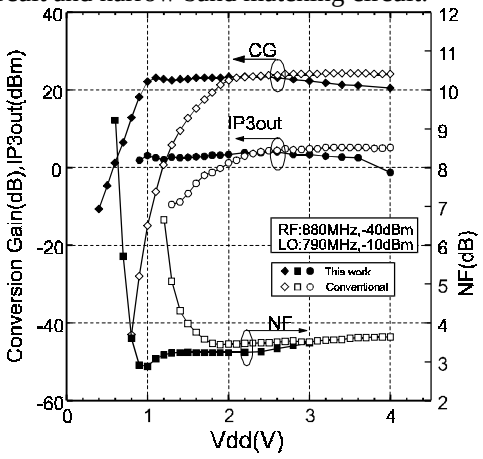

Fig.8 RF characteristics of the front-end IC as a function of the supply voltages

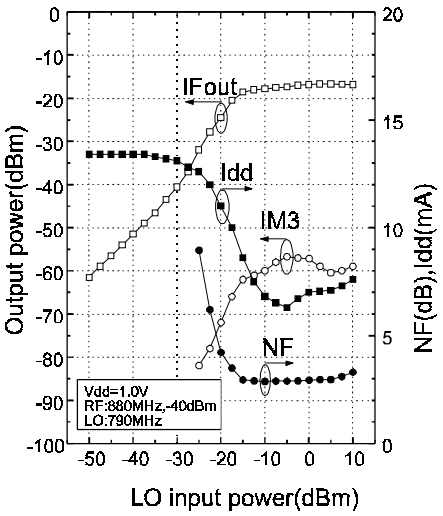

Fig.9 RF performance of the fabricated IC as a function of LO input power

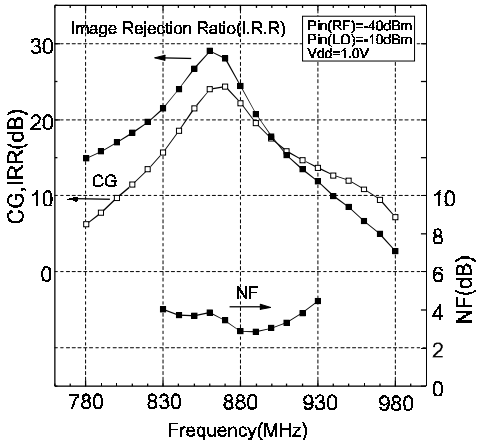

Fig.10 Frequency responses of the fabricated IC

We also evaluated this IC at 1.9GHz. Figure11 shows an input-output characteristics at 1.9GHz. The output intercept point for third-order intermodulation distortion is 0dBm.

Typical performances of the IC are summarized in table 1.

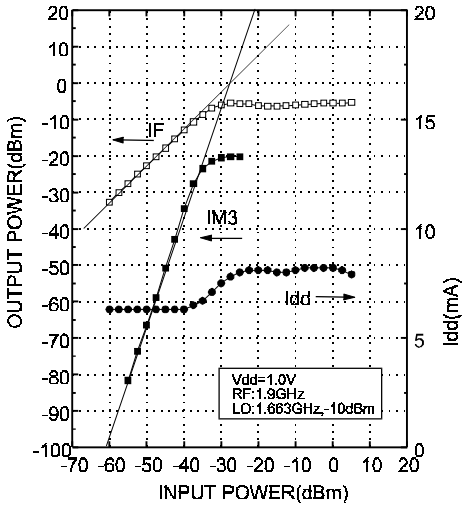

Fig.11 Pin-Pout linearity of the fabricated IC at 1.9GHz

Table 1. Performance of the front-end IC

Frequency	880MHz	1.9GHz
Dissipation Current	6.8mA	6.5mA
Conversion Gain	23.0dB	20.0dB
Noise Figure	2.8dB	3.7dB
Image Rejection Ratio	>20dB	>20dB
IP3(output)	+3.0dBm	0dBm
LO to RF isolation	25dB	20dB
Chip Size	0.75mm x 0.75mm	
Supply Voltage	1.0V	

Conclusions

A low voltage operation GaAs receiver front-end IC has been developed for mobile communication equipment. We adopted the novel E/D amplifier, D/E mixer, and high performance GaAs BP-MESFET and on-chip high-ε_r capacitors for low voltage operation at low dissipation current. Accordingly, this IC showed excellent RF characteristics of CG of 23dB, NF of 2.8dB, IP3out of +3.0dBm and low dissipation current of 6.8mA under the extremely low supply voltage of 1.0V,at 880MHz. The IC also shows excellent RF characteristics at 1.9GHz with dissipation current of 6.5mA . This IC is mounted in the small size surface mount plastic package. This new IC will contribute to realize the operation using "one battery cell" (1.2V).

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References

[1] O.Ishikawa et al., "Advanced technologies of Low-power GaAs ICs and Power Modules for Cellular Telephones", IEEE GaAs IC Symposium. Tech. Dig. pp131-134, 1992.

[2] M.Sagawa et al., "Radio Frequency Integrated Circuits for Portable Telephone Terminal", MWE 92 Workshop Dig., pp.159-165.

[3] H.Sakai et al., "Low Power GaAs IC's for Mobile Communication Equipment", GaAs and Related Compounds, 1992.

[4] J.Itoh et al., "Miniaturized Receiver Front-End Hybrid ICs for Mobile Communication Equipment using Flip-chip Bonding Technology", 1995 MTT-S International Symposium Tech. Dig., pp.15-20, Feb.1995.

[5] K.Takahashi et al., "Miniaturized Hybrid ICs for Mobile Communication Equipment using Flip-Chip Bonding Technology", IEICE Tech. Rep. MW93-158, pp.75-80.

[6] T.Nakatsuka et al., "A Highly Miniaturized Receiver Front-end Hybrid IC Using On-chip High-Dielectric Constant Capacitors for Mobile Communication Equipment", MMWMCS Tech. Dig., pp. 85-88.1995.

[7] M.Nakatsugawa et al., "An L-Band Ultra Low power Consumption Monolithic Low Noise Amplifier", IEEE GaAs IC Symposium. Tech. Dig., pp.45-48, 1993.

[8] Y.Imai et al., "Design and Performance of Low-Current GaAs MMIC's for L-Band Front-End Applications", IEEE Trans. Microwave Theory Tech., vol.MTT-39, pp.209-215, Feb.1991.

[9] A.Tamura et al., "WSiN/SiO_2 capped annealing for Si-implanted GaAs", J.Appl.Phys., vol.67, pp.6171-6174, 1990.

[10] M.Nishitsuji et al., "Advanced GaAs-MMIC Process Technology Using High-Dielectric Constant Thin Film Capacitors By Low-Temperature RF Sputtering Method", IEEE GaAs IC Symposium. Tech. Dig., pp.329-332, 1993.

[11] M.Shibuya et al., "Preparation of $SrTiO_3$ Films by RF Magnetron Sputtering Method," Extended Abstracts of The 53th Autumn Meeting of The Japan Society of Applied Physics 17a-ZV-10, 1992.